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IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

RAMBUS INC., Plaintiff, v. HYNIX SEMICONDUCTOR INC., HYNIX SEMICONDUCTOR AMERICA INC., HYNIX SEMICONDUCTOR MANUFACTURING AMERICA INC., SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A., Defendants.	No. C-05-00334 RMW ORDER GRANTING IN PART AND DENYING IN PART RAMBUS'S MOTION TO STRIKE; DENYING MOTION FOR SUMMARY JUDGMENT No. 1 OF INVALIDITY; AND STRIKING MOTION FOR SUMMARY JUDGMENT No. 2 OF INVALIDITY **[Re Docket Nos. 2406, 2458, 2533]**
RAMBUS INC., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SAMSUNG AUSTIN SEMICONDUCTOR, L.P., Defendants.	No. C-05-02298 RMW **[Re Docket Nos. 1251, 1286, 1327]**

RAMBUS INC., Plaintiff, v. MICRON TECHNOLOGY, INC., and MICRON SEMICONDUCTOR PRODUCTS, INC. Defendants.	No. C-06-00244 RMW **[Re Docket Nos. 1490, 1525, 1562]**

Rambus has accused the Manufacturers[1] of infringing various patents. Trial is scheduled for January 19, 2009. Pursuant to a case management deadline for filing summary judgment motions, the Manufacturers have filed two motions for summary judgment of invalidity pursuant to 35 U.S.C. § 102(b). Rambus opposes both motions. Rambus also moves to strike the two motions for violating a case management order. The court has reviewed the papers and considered the arguments of counsel. For the following reasons, the court grants Rambus's motion to strike the Manufacturers' summary judgment motion no. 2 and the court does not consider it. The court denies Rambus's motion to strike the Manufacturers' summary judgment motion no. 1. The court denies the Manufacturers' motion for summary judgment no. 1.

I. RAMBUS'S MOTION TO STRIKE

Before turning to the Manufacturers' motions for summary judgment of invalidity, the court must address Rambus's motion to strike those motions.

A. Background

On April 24, 2007, the court entered a joint case management order "to adopt special procedures for managing the complex issues and multiple parties in future proceedings" in these cases. *E.g.*, *Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334, Docket No. 174 at 1 (N.D. Cal. Apr. 24, 2007). The order included a schedule for trying Rambus's patent claims and the Manufacturers' defenses. *Id.*, at 2 & Attach. C. The schedule set deadlines for filing infringement

[1] The court collectively refers to the Hynix, Micron, Nanya, and Samsung entities in this suit as "the Manufacturers."

contentions, a joint claim construction statement, claim construction briefs, and "summary judgment motions that depend on claim construction issues." *Id.*, Attach. C. At the deadline for filing such summary judgment motions, Rambus filed motions for summary judgment of infringement and the Manufacturers filed motions for summary judgment of non-infringement and invalidity pursuant to 35 U.S.C. § 112.

The court issued another scheduling order as the trial date approached. *See* Docket No. 1963 (Jul. 16, 2008). The order set a deadline for dispositive motions. It explained that:

> Given these cases' histories, a few deadlines may require clarification. A "dispositive motion" is a motion for summary judgment that disposes of a portion of the case. The court will *not* entertain any dispositive motion that turns on an issue of claim construction. Such motions were supposed to be filed on October 5, 2007. *See* Joint Case Management Order, Attachment C (Apr. 24, 2007).

Id. at 3 (emphasis in original).

On October 24, the Manufacturers filed two motions for summary judgment of invalidity pursuant to 35 U.S.C. § 102(b). The first motion's introduction argues that:

> Rambus asked the Court to construe its claims broadly. Under the constructions it requested, and which the Court adopted, the five claims at issue on this motion indisputably read directly on the Bennett prior art. Because there is no genuine issue of fact for the jury, the Court should resolve these claims against Rambus before trial.

Docket No. 2406, 2:5-8 (Oct. 24, 2008). The second motion similarly argues that "each and every limitation of the asserted claims are present in the Novak patent. . . . There is no genuine issue of material fact regarding the disclosure of the relevant limitations in Novak." Docket No. 2458, 1:8-13 (Oct. 24, 2008).

B. Analysis

Rambus moves to strike the Manufacturers' two motions for summary judgment for violating the court's scheduling orders. The Manufacturers first argue that the motions do not "turn on issues of claim construction" because the motions "do not require the Court to resolve an issue of claim construction." The court disagrees. "[I]t is axiomatic that that which would literally infringe if later anticipates if earlier." *Bristol-Myers Squibb Co. v. Ben Venue Laboratories, Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001). The parties clearly understood that the court's order set a deadline for filing

motions for summary judgment of infringement and non-infringement that turn on the interpretation of a claim term. Anticipation involves the same inquiry as infringement; there is no reason to believe that one "turns on issues of claim construction" while the other does not.

The Manufacturers next argue that the court's order could not have contemplated its motions for summary judgment of invalidity because as of the court's deadline final invalidity contentions were not yet due and discovery had not yet closed. The Manufacturers argue that even if this interpretation is wrong, it was reasonable and their failure to file their two motions timely should be forgiven. This argument fails because there is noting inherently unfair about requiring motions that depend on how claims are interpreted to be filed before final contentions or before all discovery is completed. If the Manufacturers believed they needed additional time, they could have filed a motion asking for relief from the deadline. This argument also cannot explain why the parties acted as though motions for summary judgment of infringement and non-infringement were due in October 2007. Finally, and most importantly, the argument overlooks the court's well-known desire to grapple with issues of infringement and validity while simultaneously addressing claim construction. Indeed, the court remarked on the Manufacturers' failure to file motions for summary judgment of invalidity and the difficulties that failure created in understanding the scope of the parties' claim construction dispute. *Rambus Inc. v. Hynix Semiconductor, Inc.*, 569 F. Supp. 2d 946, 971 (N.D. Cal. 2008) ("This leaves the court to speculate as to why this dispute is material. Either this dispute is about nothing, or the Manufacturers are suggesting that the court construe a claim so broadly that it is invalid. This uncertainty defeats the purpose of the court's case management order."). If there could be any doubt about the meaning of the court's case management order, this passage in the claim construction order made it clear that the deadline for filing such motions had passed. Because the Manufacturers' interpretation of the court's order is not reasonable, the court rejects it.

Of course, a party may seek relief from a case management order upon a showing of good cause. *Zivkovic v. S. Cal. Edison Co.*, 302 F.3d 1080, 1087-88 (9th Cir.2002); *Hynix Semiconductor Inc. v. Rambus Inc.*, 250 F.R.D. 452 (N.D. Cal. 2008). The court therefore treats the Manufacturers'

motions for summary judgment as implicitly requesting relief from the court's case management orders. *Cf. United States v. 1982 Sanger 24' Spectra Boat*, 738 F.2d 1043, 1046 (9th Cir.1984) ("The moving party's label for its motion is not controlling. Rather, the court will construe it, however styled, to be the type proper for relief requested.").

The Manufacturers' first motion for summary judgment asserts that U.S. Patent No. 4,734,909 anticipates some of Rambus's claims. The Manufacturers point out that the patent was not cited in the prosecution history of Rambus's patents, and suggest that they did not discover the patent's applicability to this case until July 25, 2008. *See* Decl. of Michael Eisenberg, Docket No. 2393 ¶ 2 (Oct. 24, 2008) ("I discovered U.S. Patent No. 4,734,909 (the "Bennett Patent") on or around July 25, 2008 while reviewing prior art."). Though the Eisenberg Declaration does not clearly state that *the Manufacturers* were unaware of the Bennett patent until July 25, 2008, it does support the inference that the Manufacturers did not know of the Bennett patent when the October 2007 summary judgment filing deadline passed. *Accord* Tr. 73:20-74:25 (Dec. 10, 2008) (representations by Messrs. Berezin and Powers that the Manufacturers did not find Bennett until after October 2007). Because the Manufacturers could not have filed their motion for summary judgment with respect to the Bennett patent by the deadline set by the court, the Manufacturers have established good cause for relief with respect to the Bennett motion.

The Manufacturers do not attempt a similar showing with respect to the Novak patent, U.S. Patent No. 4,663,735. Nor could they. Multiple Rambus patents-in-suit disclose the Novak patent as a cited reference. *See*, *e.g.*, U.S. Patent Nos. 6,266,285 (page 2); 6,314,051 (page 1); 6,324,120 (page 2). The Manufacturers did not have to "discover" the Novak patent or its importance to the Farmwald/Horowitz patents-in-suit; the patent prosecution process had already done so. The Manufacturers' failure to make their arguments based on the Novak patent in a diligent and timely manner dooms their implied effort to seek relief from the case management order's deadline. *See Johnson v. Mammoth Recreations, Inc.*, 975 F.2d 604, 610 (9th Cir.1992).

Accordingly, the court denies Rambus's motion to strike with respect to the Manufacturers' first motion for summary judgment and grants Rambus's motion with respect to the Manufacturers'

second. The Manufacturers may of course make their invalidity arguments based on Novak at trial. Their failure to comply with the court's case management order, however, forfeits their right to bring a summary judgment motion and precludes them from making their Novak arguments at this juncture.

II. LEGAL STANDARD

A. Summary Judgment

Ninth Circuit law governing summary judgment procedures applies because this procedural law does not relate to substantive patent law principles. *In re Cygnus Telecomm'ns Tech., LLC, Patent Litig.*, 536 F.3d 1343, 1351-52 (Fed. Cir. 2008). Because a patent claim is presumed to be valid, the Manufacturers bear the burden of persuasion at trial as to whether or not each asserted claim is invalid. 35 U.S.C § 282. Thus, as movants, the Manufacturers bear the burden of producing evidence showing that the reference in question discloses each limitation of each claim that the Manufacturers argue is invalid.

If the Manufacturers fail to meet this burden of production, Rambus need not produce anything to defeat summary judgment. *Nissan Fire & Marine Ins. Co., Ltd. v. Fritz Companies, Inc.*, 210 F.3d 1099, 1102-03 (9th Cir. 2000). If the Manufacturers satisfy this burden of production, Rambus must produce evidence such that a jury, drawing all inferences in favor of Rambus, could find that the reference does not anticipate the claim at issue. *Id*. If Rambus produces such evidence, the motion must be denied. *Id.* A failure by Rambus to adduce such evidence, however, entitles the Manufacturers to summary judgment. *Id.*

A mere disagreement between experts is not sufficient to raise a triable issue of fact. An expert's opinion must be supported by facts to support or defeat a motion for summary judgment. The Federal Circuit has held that an expert's "unsupported conclusion" as to whether there is infringement or whether a claim limitation is satisfied is not sufficient. *Arthur A. Collins, Inc. v. N. Telecom Ltd.*, 216 F.3d 1042, 1046-48 (Fed. Cir. 2000). Instead, the expert must "set forth the factual foundation for his opinion – such as a statement regarding the structure in the accused product – in sufficient detail for the court to determine whether that factual foundation would

support a finding of infringement under the claim construction adopted by the court, with all reasonable inferences drawn in favor of the non-movant." *Id.* at 1047-48. This requirement is not unique to the issue of infringement. It is based on Rule 56(e)(1)'s requirement that supporting or opposing declarations "be made on personal knowledge, set out facts that would be admissible in evidence, and show that the affiant is competent to testify[.]" Thus, the stringent requirement discussed in *Arthur A. Collins* applies equally to motions addressing invalidity. This standard is important here because the parties rely solely on the declarations of their technical experts to support or oppose the Manufacturers' motion for summary judgment.

B. Anticipation

A patent claim is invalid if the claimed invention was described in a printed publication more than a year prior to the patent's application date. 35 U.S.C. § 102(b). Here, the parties agree that the Bennett patent is a printed publication and that it predates by more than one year the filing of the original application for all of the claims-in-suit. The only dispute is whether the Bennett patent describes each of the claimed inventions.

This dispute raises a question of fact. *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991). A reference anticipates a claim if it includes *all* of the claim's elements or limitations. *Id.* The reference's disclosure of each limitation need not be explicit; a limitation may be inherently disclosed if the prior art "necessarily functions" in accord with the inherent limitation. *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005). Frequently, this occurs because "[a] patent need not teach, and preferably omits, what is well known in the art." *Spectra-Physics, Inc. v. Coherent, Inc.*, 827 F.2d 1524, 1534 (Fed. Cir. 1987). This is not to suggest, however, that an inherently disclosed limitation *must* be well-known to one of ordinary skill. *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) ("Inherency is not necessarily coterminous with the knowledge of those of ordinary skill in the art.").

In practice, the anticipation inquiry is identical to the infringement inquiry, albeit with a clear and convincing standard of evidence. *Bristol-Myers Squibb*, 246 F.3d at 1378. Though it is a question of fact, anticipation, like infringement, is amenable to summary judgment where there is no

issue of material fact regarding the reference's disclosure. *Scripps*, 927 F.2d at 1576; *see, e.g., Golden Bridge Tech., Inc. v. Nokia, Inc.*, 527 F.3d 1318 (Fed. Cir. 2008) (affirming summary judgment of anticipation); *Leggett & Platt, Inc. v. VUTEk, Inc.*, 537 F.3d 1349 (Fed. Cir. 2008) (same). This suggests that summary judgment may often be appropriate due to the scarcity of genuine disputes over the content of a disclosure or operation of a device. Nonetheless, "[t]rial by document is an inadequate substitute for trial with witnesses, who are subject to examination and cross-examination in the presence of the decision-maker." *Scripps*, 927 F.2d at 1578. This admonition carries particular weight with respect to this motion because of the age (over 26 years old), size (hundreds of pages), and complexity of the allegedly anticipating reference. Where no testimony explains the contents or context of this reference, the court declines to enter summary judgment. *Cf. Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1068-69 (Fed. Cir. 2005) ("Unsubstantiated attorney argument regarding the meaning of technical evidence is no substitute for competent, substantiated expert testimony. It does not, and cannot, support [a party's] burden on summary judgment."); *Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1353 (Fed. Cir. 2001) (rejecting the argument that "that [defendants are] under no obligation to explain their theories of invalidity" and holding that "[i]t is not the trial judge's burden to search through lengthy technologic documents for possible evidence").

III. THE BENNETT PATENT

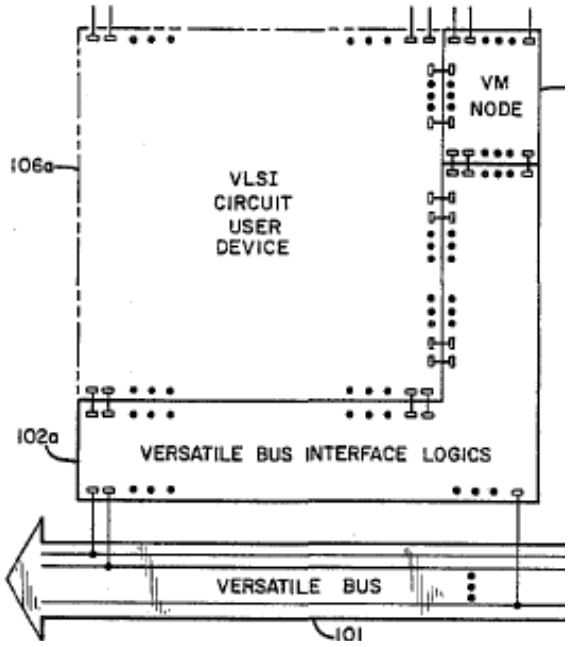
The Manufacturers must establish facts that show that the Bennett patent discloses each limitation of each claim that the Manufacturers argue is invalid. To meet their burden, the Manufacturers rely on their technical expert Joseph McAlexander, an electrical engineer, to explain DRAM technology and the voluminous Bennett patent. Rambus relies on its technical expert, Robert J. Murphy, also an electrical engineer, to rebut the Manufacturers' showing. Because the Manufacturers must make a *prima facie* showing that the Bennett patent discloses each limitation of a claim, the court's analysis begins with the Manufacturers' proffer of evidence as to each allegedly invalid claim.

A. An Overview of the Bennett Patent

U.S. Patent No. 4,734,909 (hereinafter "Bennett") uses 254 pages of figures and 282 columns of text to disclose a versatile bus interface. Due to the complexity of the information it contains, some basic overview is necessary.

1. The Versatile Bus Interface and Configuration Register

The Bennett inventors sought to provide "a scheme and an apparatus of bused digital communications interconnection, especially as between numbers of very large scale integrated (VLSI) circuit devices [with so many virtues] that it will become an interface standard embraced by diverse designers of myriad devices." Bennett, col. 12, ll. 14-25. The new interface placed its logic directly "upon the same chip substrate" as the very large scale integrated circuit (VLSIC) devices that it connected. *Id.*, col. 12, ll. 28-32. The interface consisted of a set of pins that connected to the Versatile Bus and an optional second set of pins that connect to a maintenance processor that supplies, among other things, initial settings for each VLSIC device. *Id.*, col. 12, ll. 32-45. This placement of the Bennett interface on the same chip as the VLSIC device is shown in the block diagram (a cropped version of Figure 1 of the patent) at right. The VLSIC device appears in the upper left, while the first set of pins consisting of the bus interface appear on the bottom (and connect to the bus) while the optional, second sent of pins appears in the upper right (and do not connect to the bus).



An important goal of the inventors was to create a flexible interface. *Id.*, col. 15, l. 22 - col. 17, l. 54; col. 35, ll. 31-34. The Versatile Bus maintained a standard voltage level and clock frequency, but permitted a variety of other features to be configured to meet a designer's wishes. *Id.*, col. 35, ll. 34-44. It accomplished this by placing a configuration register on each device in the environment. *Id.*, col. 35, ll. 44-51. The configuration register could be set when the device was

made (and then never changed). *See id.*, col. 35, ll. 48-50. Alternatively, the configuration register could connect to a maintenance processor through the optional second set of pins (the "VM Node maintenance interface"). *Id.*, col. 35, ll. 50-54. This second interface to the maintenance processor permitted the configuration register to be set or reset as desired. *Id.*

The preferred embodiment of the Versatile Bus interface required 37 pins to connect each VLSIC device in the environment to a Versatile Bus, though the interface permitted devices to employ as few as 3 pins and still access the Versatile Bus. *Id.*, col. 36, ll. 62-68;[2] col. 45, l. 49 - col. 46, l. 17. Eight basic parameters (or "primitives") governed the interface. *Id.*, col. 37, l. 63 - col. 38, l. 35. The parameters were: (1) number of arbitration lines per group (and pins so devoted); (2) number of arbitration groups; (3) arbitration choices; (4) number of slave ID/function parameters (and pins so devoted); (5) number of slave ID/function cycles; (6) number of wait lines (and pins do devoted); (7) number of data lines (and pins so devoted); and (8) number of data bits. *Id.*, col. 38, ll. 21-35.

Each primitive was set by the value of three binary cells in the configuration register (thus permitting each parameter to have up to 2^3 or 8 settings). *Id.*, col. 38, ll. 56-60. In other words, the configuration register contained 24 binary cells that contained the values of the eight interface parameters. *See id.* As discussed, the register could be hard-wired with certain parameter values. *Id.*, col. 38, ll. 61-65. The inventors preferred, however, to connect the configuration register's 24 cells through the VM Node interface to the maintenance processor to allow these values to be changed. *Id.*, col. 38, l. 64 - col. 39, l. 9.

Throughout the Bennett patent, the inventors refer to different Versatile Bus configurations by an 8-digit string of numbers, with each digit ranging from one to six. For example, the preferred

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[2] The inventors considered existing package technology of the time and envisioned placing three distinct and complete interfaces on each device to permit the device to connect to three different busses. *Id.*, col. 36, ll. 62-68. This explains the inventors' later comment that "a VLSIC chip has on the order of 100 pins." *Id.*, col. 66, ll. 65-68. In that portion of the Bennett specification, the inventors remarked that adding a pin to receive a clock signal was a negligible addition to the complexity of the device. *See id.* Their discussion assumed that the VLSIC device maintained three separate bus interfaces.

embodiment of the Versatile Bus is 55255355. *See, e.g.,* col. 38, ll. 48-50. Each digit of the eight-digit string refers to the value of one of the eight interface parameters or primitives. The key to interpreting the values of each primitive appears in Figure 3 of the Bennett patent. Thus, the fourth digit (slave ID/function lines) dictates how many pins the device has dedicated to sending slave ID and function information; it ranges from "multiplexed" (with arbitration and wait information) when the value is 1 to eight dedicated pins when the value is 5 (as it is in the preferred embodiment). *See id.*, Fig. 3. Likewise, the seventh digit dictates the number of data pins and ranges from one (parameter value of 1) to 16 (parameter value of 5). *Id.*

It is critical to note that devices in the Versatile Bus interface system need not possess the maximum range of functionality. *See id.*, col. 37, l. 60 - col. 38, l. 5. Any device that can accommodate a certain value of a primitive can also operate at all lower values. *Id.* Thus, a device designer could build a device with as many as 16 data pins, but that device could operate using only one of the data pins if the Versatile Bus environment so required. What made the Versatile Bus "versatile" was that it was "always possible to find a value for each primitive that [was] supported by all the chips that are to be used together, and therefore there [was] always some Versatile Bus configuration that will allow their interconnection." *Id.*, col. 38, ll. 1-6.

A final word on the interplay between parameters VII and VIII is necessary to understand the parties' invalidity arguments. As discussed, parameter VII dictates the number of data pins that will be used in the Versatile Bus configuration. *See id.*, col. 16, ll. 59-63. Parameter VIII dictates the number of data bits in a single data word. *Id.*, col. 16, ll. 63-68. These parameters depend on each other; they are not independent because Parameter VIII depends on Parameter VII. *Id.*, col. 17, ll. 1-19; col. 82, ll. 10-16. The number of data lines (Parameter VII) must be less than or equal to the number of bits in a data word (Parameter VIII). *Id.*, col. 82, ll. 10-16. In practice, the Bennett patent's illustrations overwhelmingly configure parameters VII and VIII to the same value to ensure that the entire data word can be transferred in one clock cycle. *See, e.g., id.*, col. 85, l. 67 - col. 86, l. 4 (same values in multiplexed operations illustrations); col. 92, l. 32 - col. 96, l. 42 (same value in every sample memory operation). Nonetheless, the number of data lines can be less than the number

of bits in a data word. *See id.*, col. 17, ll. 1-31. In such situations, the number of data lines multiplied by the number of clock cycles needed for data transfer must equal the number of bits in a data word. *See id.*, col. 17, ll. 12-16. In other words:

Parameter VII x number of clock cycles for data transfer = Parameter VIII

Because of this constrained relationship between Parameters VII and VIII, the Bennett inventors refer to the Parameters as determining a "configuration dimension" that they title "data format." *See id.*, col. 16, l. 59 - col. 17, l. 31. Significantly, the "data format" parameters do not dictate the length of any block operations; they simply determine how many data pins are used and the length of a data word. *Id.*, col. 17, ll. 29-31.

2. Memory Operations

"Many, if not most, applications of VLSIC technology are likely to include memory devices." Bennett, col. 90, ll. 43-44. To avoid a "proliferation" of disparate memory interfaces, the Bennett inventors proposed a basic set of memory operations in the Versatile Bus interface environment. *See id.*, col. 90, l. 43 - col. 92, l. 8. Among the "relatively small set of operations," the Bennett inventors included basic read and write operations and block read and block write operations. *Id.*, col. 91, 6-68. Figure 32 of the Bennett patent (reproduced below) illustrates a basic read or write operation. The y-axis shows time in clock cycles, advancing downward. *Id.*, col. 92, ll. 52-54. The horizontal axis shows the preferred embodiment 37-pin bus interface on a device. *Id.*, col. 92, ll. 54-56. Boxes show activity on the corresponding pins.

The two leftmost pins (BEGIN and BUSY) indicate the status of a bus transaction. *Id.*, col.

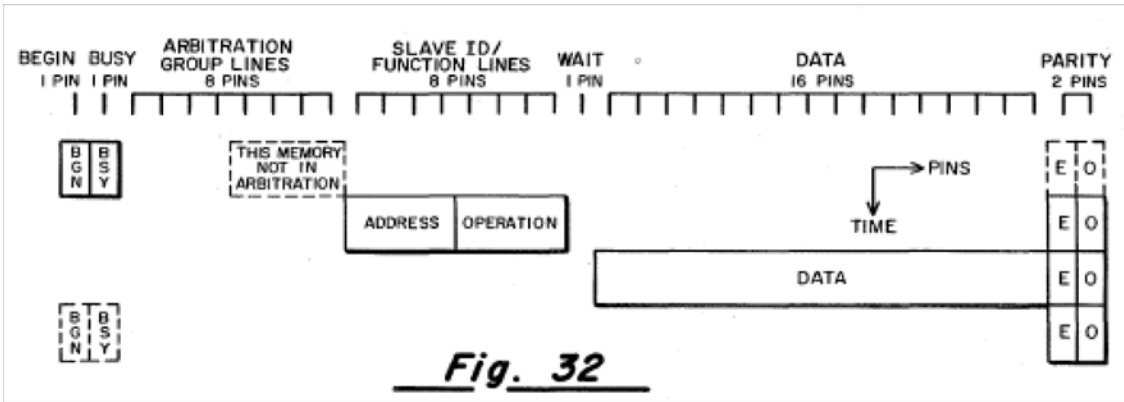

Fig. 32

46, l. 53 - col. 47, l. 17. The BEGIN signal going high indicates the start of a transaction. *Id.* The BUSY signal effectively means "the bus will be busy next cycle." *See id.* When the BUSY signal is high, the transaction is ongoing; when it goes low, the transaction terminates on the next clock cycle. *See id.* In this simple memory operation, the BUSY signal remains low, indicating that a second operation (not shown) could begin on the next clock cycle. *Id.*, col. 92, ll. 56-63.[3] The memory device in this sample operation is a slave device (i.e., it cannot take control of the bus) and it therefore ignores the simultaneous signals sent over the arbitration bus lines. *Id.*, col. 92, l. 63 - col. 93, l. 1.[4]

On the second clock cycle, the memory device receives address and "operation" information over the slave ID/function pins. *Id.*, col. 93, ll. 12-26. In this sample operation, the inventors partition the field of information equally (and arbitrarily) into address and operation. *Id.* This example implicitly contemplates a small enough memory that four bits of address information suffice to identify which memory array to read data from or write data into. *See id.* Having selected the address in memory and determined the type of operation, the memory device can send or receive

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[3] The memory devices in the Bennett system can accomplish different aspects of multiple operations simultaneously. In other words, the Bennett memory devices "pipeline" operations, leading to higher bus utilization and faster operation.

[4] Activity is shown on only 4 of the arbitration pins because the Versatile Bus configuration of this example is a 42252255, a lower configuration than the preferred embodiment configuration. *Id.*, col. 92, ll 31-36. As shown in Figure 3, a parameter I value of 4 implies that there are only 4 arbitration pins connecting to the bus.

data on the third clock cycle and effectively[5] complete the transaction. *Id.*, col. 93, ll. 27-28.

The sample operation shown above occurred in a 42252255 bus configuration. Figure 33 depicts a similar sample operation, but this time in a 43112244 bus configuration. *Id.*, col. 93, ll. 56-58. The configuration is meant to highlight the Versatile Bus's capacity to multiplex various types of information. *See id.*, col. 93, l. 56 - col. 94, l. 8. For example, parameter IV (the number of slave ID/function lines) is equal to one, i.e., it is programmed to multiplex slave ID and function information over the data lines. *Id.* Parameter VII is equal to four, i.e., the configuration uses eight data lines. *See id.* When the slave ID/function information is multiplexed, the system transmits slave ID/function information over Parameter VII's number of data lines. *Id.*, col. 94, ll. 2-5. This produces the sample memory operation shown below (using the same x-axis as Figure 32):

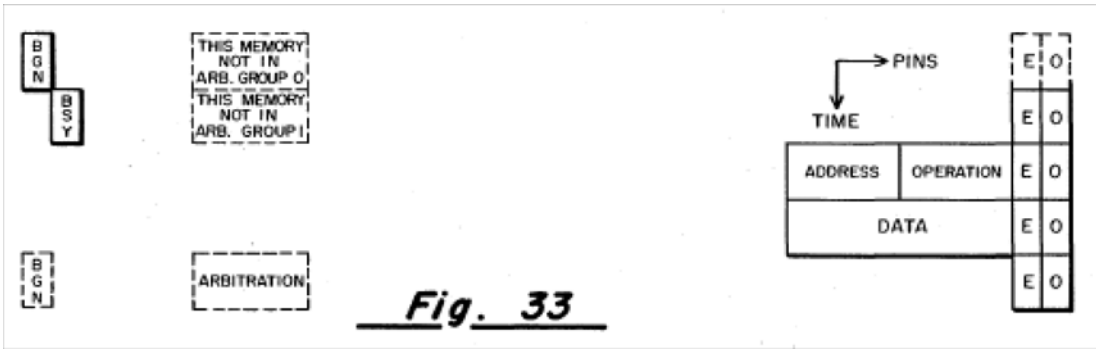

Fig. 33

As desired, the slave ID/function information arrives at the memory device over the configuration's eight data pins. The memory device sends or receives data on the following clock cycle. As in the prior configuration, parameter VI (the number of wait lines) is set to 2, i.e., "no wait lines are employed." *Id.*, col. 94, l. 2.

3. Block Memory Operations

The Versatile Bus interface also supported "block" read and write operations. Instead of transferring a single data word, block operations permitted an operation that could continue indefinitely. *See id.*, col. 17, ll. 19-29 (noting that the potential for "millions of data words" to flow

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[5] The rightmost pins convey parity information that allows the devices to check for errors in the transmission of information. The parity bits lag their corresponding information by one clock cycle. *Id.*, col. 93, ll. 28-46. Thus, even after the data is sent or received on the third clock cycle, parity information related to the data is being sent on the fourth clock cycle.

as block data "most emphatically" lacks relationship to the values of Parameters VII and VIII). To trigger a block operation, the master sent an address and an integer to the memory device. *Id.*, col. 91, ll. 54-55. In a read operation, the memory device transmitted the first data word from the address. *Id.*, col. 91, ll. 56-57. The memory device then added the integer to the first address to obtain a second address and transmitted the second data word from the second address. *Id.*, col. 91, ll. 57-59. The memory device continued to operate in a loop by adding the same integer to the most recent address and transmitting data words indefinitely. *See id.* The block read operation only terminated when the master deactivated the BUSY line. *Id.*, col. 91, ll. 56-61. A similar protocol of adding an integer to the most recent address permitted block write operations. *Id.*, col. 91, ll. 62-68.

4. The WAIT Signal's Role in Operations

In the Versatile Bus configurations discussed above, parameter VI (the number of wait lines) was set to 2, which corresponds to omitting the WAIT signal from the configurations. *See* Bennett, Fig. 3. In configurations that omit a wait line (parameter VI equal to 2), slave devices must accept transactions. *Id.*, col. 77, ll. 26-29. The inventors' preferred embodiment of the Versatile Bus interface either excluded the WAIT line or included a single pin for transmitting WAIT information. *Id.*, col. 76, ll. 1-4. The general purpose of the WAIT signal is to allow a slave device to signal to the master device that it is not "absorbing" the information being sent in the pending transaction. *Id.*, col. 76, ll. 24-30. A WAIT signal of zero informs the master that the slave device will accept the transaction. *Id.*, col. 75, ll. 62-65. A WAIT signal of one (or high) indicates a problem, but the inventors left the precise meaning of the WAIT signal open to future system designers, with a few suggested conventions. *Id.*, col. 76, ll. 7-24.

The decision to multiplex the WAIT signal or to send it over a separate pin can have a curious impact on the overall timing of operations. This impact appears in Figures 25a and 25b, reproduced below:

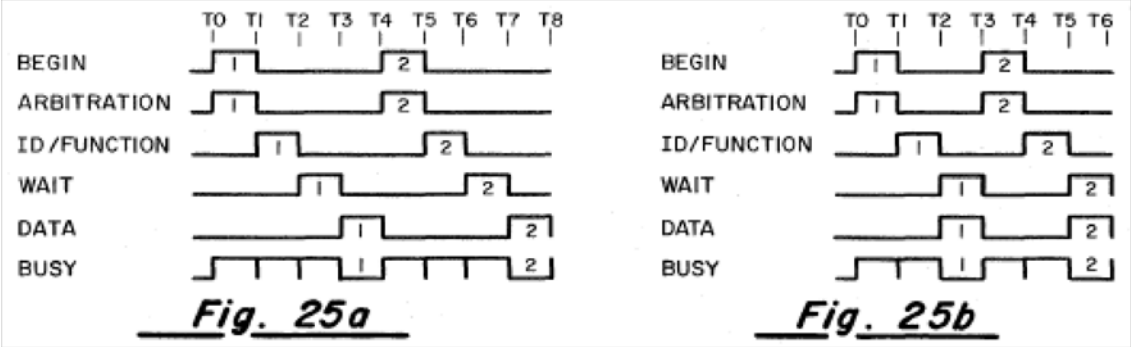

Figure 25a depicts a Versatile Bus configuration of 122121XX. *Id.*, col. 85, ll. 49-59. Parameters I, IV, and VI all equal 1, meaning that arbitration, ID/function, and wait information are all multiplexed over the data pins. *See id.*, col. 86, ll. 4-9. Fig. 3. Parameters II and V are selected to ensure that the arbitration and ID/function phases of an operation each require one clock cycle. *Id.*, col. 85, l. 67 - col. 86, l. 4. Likewise, setting parameter VII to equal parameter VIII ensures that all data is transferred over one clock cycle. *Id.* Thus, a completely multiplexed operation takes four complete cycles: one for arbitration, one for ID/function, one for wait information, and one for data. *Id.*, col. 86, ll. 27-30.

Figure 25b depicts the timing of an operation with configuration 122123XX. *Id.*, col. 85, ll. 31-41. The only difference in the configuration is the change in parameter VI from 1 to 3. In other words, Figure 25b uses a dedicated wait pin instead of multiplexing wait information over the data lines. *Id.* This permits the slave devices to transmit wait information at the same time that data is transmitted, reducing the total operation time to three clock cycles. *Id.*, col. 86, ll. 37-41.

B. Claim 16 of U.S. Patent No. 6,266,285

1. The Asserted Claim

The Manufacturers assert that the Bennett patent anticipates claim 16 of U.S. Patent No. 6,266,285. The claim generally recites a method of operating a memory device involving: (1) receiving an external clock signal, (2) receiving a delay time value and storing it in a register, (3) receiving a request for a write operation, and finally (4) sampling data in response to the write operation after the delay time transpires. Rambus colloquially refers to this claim as covering the

implementation of programmable write latency. The full text of the claim follows, with the language of the claim from which it depends incorporated in brackets:

> [[A method of operation in a memory device having a section of memory which includes a plurality of memory cells, the method comprising:
>
> receiving an external clock signal;
>
> receiving a request for a write operation synchronously with respect to the external clock signal; and
>
> sampling data, in response to the request for a write operation, after a programmable number of clock cycles of the external clock signal transpire.]]
>
> [further including storing a value which is representative of the programmable number of clock cycles of the external clock in a programmable register on the memory device.]
>
> further including receiving a set register request, wherein in response to the set register request, the memory device stores the value in the register.

2. The Evidence With Respect to Each Limitation

In this section, the court determines whether the Manufacturers have met their burden of producing clear and convincing evidence showing that the Bennett patent discloses each limitation of claim 16. The court also determines whether Rambus has rebutted this showing and whether the Manufacturers have carried their burden of persuasion with respect to each limitation.

a. A Memory Device

Mr. McAlexander states that the Bennett patent discloses a memory device. Lee Decl., Ex. 3 at C-7 (hereinafter "Bennett Chart"). He points to various portions of the Bennett patent that describe the different users of the patent's new bus interface. *See id.* For example, the Bennett patent describes its interface as "intended to be built with a CPU, IOC, Memory, or similar User device for signal and data exchange." Bennett, col. 35, ll. 60-62. The Bennett patent again defines a "User" in its bus interface as "the logics (e.g., a central processor or a memory or whatever) which communicates through the Versatile Bus Interface Logics, such as are taught by this specification, onto the Versatile Bus." *Id.*, col. 40, ll. 52-55. The Bennett patent further lists the memory operations that must be defined in the bus interface to "avoid a flexibility stifling proliferation of memory interfaces." *See id.* col. 90, l. 42 - col. 92, l. 8.

Mr. McAlexander further asserts that "[t]he VLSI memory device of Bennett necessarily includes memory cells." Bennett Chart, C-7. Mr. McAlexander does not explain why, but this is clear from the nature of memory devices and would be immediately clear to one skilled in the art. A "memory cell" stores a single bit of information. The Bennett patent discusses memory operations involving accepting addresses to different portions of the memory. *See, e.g.,* Bennett, col. 91, ll. 54-61 ("The first word is read at the specified address. The subsequent words' addresses are found by adding the integer to the address of the most recently read word."). The need for multiple addresses implies a memory with a "plurality" of memory cells.

Rambus disagrees that Bennett discloses a "memory device" as construed by the court. Rambus urges that a person of ordinary skill in the art would read Bennett and understand that it "did not intend for the memory devices used with its invention to be implemented as VLSIC devices." Opp'n at 2-3. Rambus supports this assertion by reference to a declaration from Mr. Murphy.

Mr. Murphy first points to a discussion in Bennett referring to an example of operations with large memories. There, Bennett discusses the possibility of transmitting information to a "large memory of up tp 2^{32} addresses of 32 bit words[.]" Bennett, col. 95, ll. 58-59. Mr. Murphy points out that even today (26 years after the Bennett patent application was filed) no single chip can hold that amount of memory. Murphy Decl., Ex. A ¶ 4 (hereinafter "Murphy Report"). Mr. Murphy opines that in 1982 such a memory of that capacity would fill a medium-sized room and comprise thousands of memory cards. *Id.* Therefore, Mr. Murphy believes that a person of ordinary skill in the art would not understand Bennett's "memory devices" as existing on a single VLSIC chip.

Mr. Murphy supports his position by latching onto Bennett's discussion of the theoretical maximum-size memory device that its Versatile Bus could accommodate. But read in the context of the patent, it is clear that the discussion of this "large memory" is meant to illustrate the flexibility of the bus interface, not to suggest that Bennett contemplates that all memory devices designed for use in its system should be so large. Rambus's emphasis on Bennett's discussion of "large memories" also fails to account for Bennett's discussion of memory operations with "relatively small fast

memories." *See* Bennett, col. 92, l. 11 - col. 94, l. 23. Mr. Murphy's report ignores this discussion. When asked at the hearing about the distinction between Bennett's "small fast" memories and its "large memories," Rambus answered, "a small fast memory is also a memory board but not containing as many chips and so capable of faster operation than what Bennett refers to as a large memory." Tr. 100:15-22 (Dec. 10, 2008). Because Mr. Murphy does not establish this distinction, Rambus attempted to support this distinction by repeating two arguments, which the court rejects in detail below. Thus, even if Rambus has raised an issue of fact as to whether Bennett's "large memory" devices are not the "memory devices" of Rambus's claims, Rambus has not raised an issue of fact as to whether the Bennett patent discloses "small fast" memories that are the "memory devices" of Rambus's claims.

The rejected arguments mentioned above both result from reading short passages of the specification and ignoring their context. Mr. Murphy points out a discussion in the background section of the patent where the inventors wrote that "[a]n efficient interconnect system cannot saddle simple interconnects with the coordination overhead required for the complex ones." Murphy Report ¶ 5 (citing Bennett, col. 8, ll. 10-12). Mr. Murphy states that "simple interconnects" refers to memory chips, and therefore the Bennett patent's discussions of "memories" must exclude simple memory chips. *Id.* Mr. Murphy misconstrues the Bennett patent. In this discussion, the Bennett inventors explain the basic problems that must be solved by an ideal bus interface. *See generally* Bennett, col. 7, l. 22 - col. 8, l. 12. One feature of an efficient bus interface (to the Bennett inventors) is low overhead, i.e., not "saddling" simple devices with complex interfaces. The Bennett inventors therefore disclosed a flexible system that operates at the lowest common denominator configuration, but that can operate at high levels of complexity if the device environment only includes complex devices. Mr. Murphy errs by equating this problem to be solved by the invention with a limitation on the memory devices that use the inventive bus interface.

Mr. Murphy next points out that memory chips in 1982 "had on the order of 16 pins." Murphy Report ¶ 6. He then notes that Bennett discloses that a VLSIC chip "has on the order of 100 pins." Bennett, col. 66, ll. 65-66. Mr. Murphy concludes that a person of ordinary skill in the art

would therefore conclude that the Bennett inventors could not have meant to add the Versatile Bus interface to a memory and increase the pin count so much. Murphy Report ¶¶ 6-8. But as discussed above, the Bennett patent's reference to "on the order of 100 pins" was made in the context of considering existing microprocessor packages. Bennett frequently stresses that the preferred embodiment requires 24 pins for the VM Node interface and 37 pins for the preferred Versatile Bus interface. This total of 71 is not trivial, but the Bennett inventors frequently refer to implementing the Versatile Bus interface with as few as three pins and minimizing the number of pins needed for the VM Node interface. *See* Bennett, col. 118, ll. 15-28 (explaining that adding logic to the devices would reduce the need for VM Node interface pins, but that "reduction of pins . . . is not the subject of this application."). Thus, the preferred memory device interface has *at most* 71 pins, not "on the order of 100 pins." The "on the order of 100 pins" remark in the specification therefore has no bearing on the scale of Bennett's memory devices.

Mr. Murphy is correct in pointing out that it would be expensive to make memory chips that implement the Versatile Bus interface. But his focus on the expense of implementing the Versatile Bus interface on a memory device is irrelevant. "A reference is no less anticipatory if, after disclosing the invention, the reference then disparages it." *Celeritas Techs., Ltd. v. Rockwell Int'l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998). It follows that the expense of producing or implementing an anticipatory reference is also irrelevant.

Finally, it bears noting that the Bennett inventors were aware of memory cards and referred to them as such when they chose. *E.g.,* Bennett, col. 37, ll. 26-36. The inventors disparaged the existing computer busses and the "many cards [that] can be placed on the bus and communicate among themselves." *Id.*, col. 37, ll. 26-28. The Bennett inventors hoped that a versatile bus connecting VLSIC chips could omit the "multiunit handshaking that is just so much excess baggage" found in existing busses. *Id.*, col. 37, ll. 37-41.

In sum, it is clear that the Bennett inventors sought to disclose a bus interface for use between VLSIC devices, including memory devices. Whether the Versatile Bus interface would have been an expensive addition to such memory chips is irrelevant. The court therefore concludes

that the Manufacturers have carried their burden of producing evidence that Bennett discloses a memory device, and that Rambus has failed to rebut this showing.

b. Receiving an External Clock Signal

The next limitation of claim 16 requires the memory device to receive an external clock signal. Mr. McAlexander states that the Bennett patent discloses such a clock signal. Bennett Chart, C-7. He points out that the Versatile Bus interface transmits "[a] clock of approximately equal phases, both within each [sic] 40 nanoseconds, . . . to every interfacing chip on a versatile Bus." Bennett, col. 51, ll. 65-67. Bennett describes in detail the need to choose between a synchronous or asynchronous bus protocol. *Id.*, col. 66, ll. 10-18. After disparaging the existing asynchronous protocols, *see id.*, col. 66, ll. 19-58, the Bennett inventors opted for "a clocked, or synchronous, protocol." *Id.*, col. 66, ll. 59-60. The Manufacturers have therefore met their burden of showing that the Bennett patent discloses "receiving an external clock signal." Rambus does not dispute that the devices featuring the Versatile Bus interface receive an external clock signal. The court therefore concludes that the Manufacturers have shown that the Bennett patent discloses this limitation of claim 16.

c. Receiving a Request for a Write Operation

The method of claim 16 also requires the memory device to "receiv[e] a request for a write operation synchronously with respect to the external clock signal." Mr. McAlexander states that the memory devices in the Versatile Bus interface operate in this manner. Bennett Chart, C-8. Indeed, the Bennett patent's interface employs two clock signals, φ1 and φ2, to create a reference signal "to which all communication between the Versatile Bus Interface Logics and the User, and upon the Versatile Bus, is referenced." Bennett, col. 101, ll. 50-54. Furthermore, all signals from the interface logic to a user device (like a memory device) are triggered by the leading edge of one of the clock signals. *See id.*, col. 102, ll. 9-27. As discussed above, various types of requests for a write operation can be sent in the slave ID/function block and received by the Bennett memory devices. The Manufacturers have therefore met their burden of showing that the Bennett patent discloses "receiving a request for a write operation . . . ." Rambus does not dispute that the devices

featuring the Versatile Bus interface synchronously receive requests for a write operation. The court therefore concludes that the Manufacturers have shown that the Bennett patent also discloses this limitation of claim 16.

d. A Programmable Number of Clock Cycles

The next two limitations of the method of claim 16 require the memory device to "sampl[e] data, in response to the request for a write operation, after a programmable number of clock cycles of the external clock signal transpire" and for the memory device to "stor[e] a value which is representative of the programmable number of clock cycles of the external clock in a programmable register. . . ." The court addresses the limitations together because the parties' dispute turns on whether Bennet discloses the sampling of data after a programmable number of clock cycles transpire.

The Manufacturers, through Mr. McAlexander, point to the following pieces of evidence. *See* Bennett Chart, C-8 & C-9. The Versatile Bus interface supports pipelining operations. Bennett, col. 46, ll. 18-20. "Pipelining" refers to breaking a bus transaction into its constituent parts. In the Versatile Bus interface, these parts comprise arbitration, slave ID/function, and wait/data. *See id.*, col. 46, ll. 23-29. The interface uses separate pins for the different types of information. *Id.* Pipelining allows the device to receive the various pieces of information on the separate sets of pins at staggered points in time. *Id.* For example, in the memory operations shown above in Figures 32 and 33, the memory device receives arbitration information on a first clock cycle or cycles, slave ID and function information on a second clock cycle, and then data information on a third clock cycle. *See id.*; Figs. 32, 33. The pipelined operations in the Versatile Bus interface can run two to ten operations deep and have a latency of two to ten clock cycles. *Id.*, col. 46, ll. 18-23. The preferred Versatile Bus interface runs a pipeline with a latency of three clock cycles. *Id.*, col. 46, ll. 21-23. It is important to note that this latency refers to the number of clock cycles between the BEGIN signal (the generic signal that indicates that a master wishes to use the bus) and the completion of the data transfer, not the latency between an operation and its completion.

With these concepts in mind, Mr. McAlexander points to the example of multiplexed

operations in Figures 25a and 25b discussed above. Mr. McAlexander notes that in the 122121XX configuration shown in Figure 25a, the total transaction time is four clock cycles. Bennett Chart, C-8. By changing the value of parameter VI from 1 to 3, i.e., by dedicating a pin to the wait signal and not multiplexing it with data, the device is able to send the wait signal while simultaneously sending or receiving data. This reduce the total transaction time to three clock cycles. *Id.* Of course, the BEGIN signal is not the "request for a write operation" received by a memory device in the Versatile Bus architecture.[6] A request for a write operation is indicated by information transmitted as part of the slave ID/function block of information. Nevertheless, in Figure 25a, there is a delay of 1 clock cycle between the memory device receiving the request for a write operation and the memory device receiving data. In Figure 25b, there is no delay between receiving the request for a write operation and the memory device's receipt of the data. This difference results from parameter VI in the configuration register being programmed to equal 1 or 3.

Rambus responds by pointing out that parameter VI does not equal the time delay between the memory's receiving a request for a write operation and sampling data. The court has already rejected this argument, though at that time it was made by Hynix. *See Hynix Semiconductor, Inc. v. Rambus Inc.*, 2008 WL 5100791, *5-*7 (N.D. Cal. Dec. 2, 2008) (rejecting Hynix's non-infringement argument with respect to the programmable register's CAS latency value).

The relevant inquiry, as dictated by the text of Rambus's claim, is whether the value is *representative* of the number of clock cycles between the write request and sampling. The court previously held that a stored value was representative of a delay time because the delay time could be expressed as a function the of the stored value. *See id.* Parameter VI (the number of wait lines used in the Versatile Bus configuration) can vary from 1 to 5. It appears that when Parameter VI

---

[6] This mistake underscores why the second example called out by the Manufacturers' in their motion does *not* illustrate a programmable delay between receiving a request for a write operation and sampling data in response. While the total transaction times in Figures 32 and 33 differ due to how the different configurations process arbitration information, both examples illustrate waiting *zero* clock cycles between receiving a request for a write operation and sampling data in response. In both examples, the memory devices receive a request for a write operation on clock cycle *t*, and sample data in response on clock cycle $t + 1$.

equals 1, i.e., when the wait line is multiplexed with the data lines, the "write latency" is one clock cycle because the data cannot be received until the wait signal is sent. It further appears that when Parameter VI equals anything else (2-5), the "write latency" is zero because the configuration either lacks a wait signal or transmits it simultaneously with the data. Obviously, this is not the clear functional relationship that connected the CAS latency value to the delay before the device began to output data in *Hynix*. But the value of Parameter VI still determines the "write latency" that will exist in the Versatile Bus interface's memory operations.

However, one value being "representative" of another requires more than a functional relationship between the two. The word "representative" implies some level of recognition by another that the first value indicates or represents the second. The verb "represent" means "[t]o bring clearly and distinctly before the mind, esp. (to another) by description" and "[t]o symbolize, to serve as a visible or concrete embodiment of (some quality, fact, or other abstract concept)." Oxford English Dictionary (2d ed. 1989) (definitions 2a and 6a). In *Hynix*, the evidence showed that the DRAMs' CAS latency value equaled the amount of time before the DRAM made information available to the bus. It was trivial from that to recognize that the CAS latency value also controlled the timing of all other aspects of the DRAM's response to a read operation, namely, when the device began to output data. Here, Mr. Murphy correctly points out that the Bennett interface's eight parameters "do not include the time delay between the receipt of a read or write command and the output or input of the corresponding data." Murphy Report ¶ 12. The Bennett inventors never referred to Parameter VI as embodying a mechanism for controlling the write latency of the Versatile Bus interface's memory operations. Drawing all inferences in favor of Rambus, the value of Parameter VI, i.e., the number of wait lines used in a configuration of the bus interface, would not be recognized as representing the number of clock cycles between receiving a request for a write operation and sampling data in response.

Two additional arguments made by Rambus deserve attention because of their tendency to "cloud rather than clarify the central legal issues" regarding Bennett and risk "draw[ing] the [jury's] attention to peripheral matters." *Allen Eng'g Corp. v. Bartell Industries, Inc.*, 299 F.3d 1336, 1356

(Fed. Cir. 2002). Rambus argues that "the values in the configuration register do not determine the actual configuration of the device." Murphy Report ¶ 13. Mr. Murphy bases this conclusion on the Versatile Bus interface's requirement that the bus configuration support the least complex device. He states that, "the actual configuration of the device will depend not just on the values in its configuration register, but also the values in the configuration registers of the other components in the system." *Id.* Rambus therefore suggests that a device could have a "3" in its register for parameter VI, but another device could have a value of "2" and the Versatile Bus environment would then operate at the lower value despite the higher value in one of the device's configuration registers. But Rambus and Mr. Murphy appear to confuse the role of the configuration register in the Versatile Bus interface when all of the devices possess programmable configuration registers. Because different devices will have different interface complexities, the maintenance processor programs *all* of the devices in such a bus environment with the same octet of values. The value in the configuration register always determines the actual configuration of the device. Rambus's example does not accurately describe the Bennett bus interface in such an environment.

Rambus also suggests that the description of Figures 25a and 25b are purely exemplary and that there is no guarantee that there is a one cycle delay between the request for a write operation and the output of data. Rambus bases this argument on Bennett's statement that "[i]n order to simplify presentation of timing concepts all Arbitration, Slave Identification/Function, and Data activities are assumed to be but one cycle." Bennett, col. 85, ll. 17-19. Rambus's argument fails for two reasons. First, this is not a baseless assumption by the Bennett inventors. The other primitives in the Figure 25 example are selected to ensure that arbitration, slave ID/function, and data all occur in one cycle. In other words, this is not a guess; there is a configuration of the Versatile Bus interface in which this is true. Second, it is irrelevant. That the arbitration, slave ID/function, and data activities are all assumed to last one cycle does not impact the amount of delay *between* the slave ID/function and data activities. That delay is determined by the status of the wait signal.

e. Set Register Request

The final limitation of claim 16 requires the memory device to receive "a set register request,

wherein in response to the set register request, the memory device stores the value in the register." Mr. McAlexander states that Bennett discloses a memory device receiving a set register request. Bennett Chart, C-9. He points out that parameter VI is programmed into the configuration register when the devices on the Versatile Bus are initialized. *See* Bennett, col. 35, ll. 48-54. He does not explain how this happens. *See* Bennett Chart, C-9.

In their brief, the Manufacturers cite a cryptic portion of Bennett that states:

> The maintenance processor effectuates the impressing of a pertinent bit pattern upon the configuration register within each Versatile Bus Interface Logics by respectively emplacing a logical Low on signal (L) SCAN/SET ENABLE, a logical Low on signal (L) SCAN/SET SELECT (L=SET), a logical High on signal (H) SEL LOOP D, and appropriate logical High or Low level of signal (H) SET DATA as a respective logical "1" or "0" is desired to be set within each bit position of Loop D as gated by clock φ2.

Bennett, col. 125, ll. 46-56. The Manufacturers provide no testimony to explain the significance of the passage, and without any testimony, the court cannot grant summary judgment.

3. Conclusion

The Manufacturers have failed to meet their burden of producing clear and convincing evidence that the Bennett patent discloses the "set register request" limitation of claim 16 of the '285 patent. The Manufacturers have failed to carry their burden of persuasion with respect to the "programmable number of clock cycles" limitations because Rambus has produced evidence in opposition that raises a triable issue of fact. Accordingly, the court denies the Manufacturers' motion for summary judgment with respect to claim 16 of the '285 patent.

C. Claim 27 of the '051 Patent

1. The Asserted Claim

The Manufacturers next assert that the Bennett patent anticipates claim 27 of U.S. Patent No. 6,314,051. The claim generally recites a memory device that possesses: (1) clock receiver circuitry for receiving an external clock signal, (2) a programmable register for storing a value representative of the device's write latency, and (3) data input circuit to sample data after the write latency period. Rambus colloquially refers to this claim as covering a device featuring programmable write latency. The full text of the claim follows:

> A memory device having a plurality of memory arrays, wherein each memory array includes a plurality of memory cells, the memory device comprising:
>
> clock receiver circuitry to receive an external clock signal;
>
> a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before sampling a first portion of data, wherein the first portion of data is sampled in response to an operation code;
>
> and data input receiver circuitry to sample the first portion of data synchronously with respect to the external clock signal.

2. The Evidence With Respect to Each Limitation

The limitations of claim 27 closely resemble some of the limitations of claim 16 of the '285 patent. In short, Rambus has raised a triable issue of fact regarding whether Bennett's memory interface's parameter VI is "representative" of "a number of clock cycles of the external clock signal" that must transpire before the memory device samples data. The court therefore denies the Manufacturers' motion for summary judgment with respect to this claim.

D. Claim 43 of the '051 Patent

1. The Asserted Claim

The Manufacturers also argue that the Bennett patent anticipates claim 43 of the '051 patent. The claim is very general, and recites a synchronous DRAM with (1) input receiver circuitry to sample an operation code synchronously and (2) input receiver circuitry to sample data in response to the operation code after a predetermined number of clock cycles. The full text of the claim follows, with the language of the claim from which it depends incorporated in brackets:

> [A memory device having a plurality of memory arrays, the memory device comprising:
>
> first input receiver circuitry to receive an operation code synchronously with respect to an external clock; and
>
> second input receiver circuitry to sample data, in response to the operation code, after a predetermined number of clock cycles of the external clock]
>
> wherein the memory device is a synchronous dynamic random access memory.

2. The Evidence With Respect to Each Limitation

The final limitation of claim 43 modifies the preambulary "memory device" limitation, so the

court addresses the two limitations together. The court discussed the arguments regarding the Manufacturers' showing that the Bennett patent discloses a "memory device" above. *See supra* § III-B-2-a.

The first difference between the two claims with respect to the "memory device" limitation is that claim 16 recited a memory device with a plurality of memory cells, while claim 43 recites a memory device with a plurality of memory "arrays." During claim construction, the parties agreed that a "memory cell" was "an electronic storage element(s) in a memory array." *Rambus Inc. v. Hynix Semiconductor, Inc.*, C-05-00334, Docket No. 254, at 3 (N.D. Cal. Jul. 11, 2007) ("Joint Claim Construction Statement"). But the parties disputed the construction of "memory array." *See id.* at Jt. App'x A, 21. Rambus argued that a "memory array" was "a plurality of data storage elements that are arranged in rows and columns." *Id.* The Manufacturers submitted that no construction was necessary. *Id.* Neither party raised the issue of the construction of "memory array" in their briefs or at the claim construction hearing. Nor did any party consider the dispute particularly significant. *See* Docket Nos. 254-4 (ranking the dispute 39th on Rambus's list of priorities), 254-5 (failing to list the dispute on the Manufacturers' list of 47 important claim construction disputes).

To the extent the term needs construction, the court agrees with Rambus's construction. The parties agree that a memory cell is a storage element in a memory array. The parties also agree that a "synchronous dynamic random access memory" is "a synchronous semiconductor memory device which includes one or more arrays of DRAM cells." Joint Claim Construction Statement, 3. Thus, the parties agree that an array contains memory cells and that a DRAM contains one or more arrays. This favors Rambus's construction, but does not necessarily explain the rows and columns limitations suggested by Rambus. The extrinsic evidence fills the gap. Memory arrays are "rectangular grids of storage cells with each cell holding one bit of data. . . . [M]emory arrays are organized into *rows* and *columns*." Bruce Jacob, Spencer W. Ng & David T. Wang, Memory Systems: Cache, DRAM, Dick 316-17 (2008). In light of the parties' agreements, the extrinsic evidence, and silence of the Manufacturers, the court adopts Rambus's construction of "memory

array."

To establish that Bennett discloses a memory device with a plurality of memory arrays, Mr. McAlexander refers to the "large memory" discussed above. Bennett Chart, C-14. In so doing, he concedes that such a large memory would have been composed of multiple chips, and that each chip would have at least one memory array. *See id.* As discussed above, Rambus has raised a triable issue of fact as to whether the "large memories" of Bennett satisfy the "memory device" limitation of Rambus's claims. While Rambus has not similarly raised a question of fact with respect to Bennett's "small fast memories," Mr. McAlexander does not state whether Bennett's "small fast" memories would have had a plurality of memory arrays. Because the Manufacturers have not produced sufficient evidence on summary judgment to establish that Bennett discloses the slightly different "memory device" of claim 43, the court cannot grant summary judgment.

The court must also deny summary judgment because the Manufacturers have not produced sufficient evidence on summary judgment that the Bennett patent discloses a memory device that is a synchronous dynamic random access memory. *See* Bennett Chart, C-16. Mr. McAlexander generally cites Bennett's seven-column discussion of memory operations as disclosing a synchronous DRAM. Those seven columns specifically mention only one type of memory: ROM or read-only memory. *See* Bennett, col. 91, ll. 1-2. Bennett discusses ROMs while explaining the limited number of operations that can be done with a memory device, and it does so to point out that memories like ROMs cannot receive write operations. *See id.* Bennett's discussion thus impliedly discloses some type of memory device that can receive write operations. The jury will have to determine at trial whether that implied disclosure encompasses a dynamic random access memory.

Because the court denies the Manufacturers' motion for summary judgment with respect to claim 43 for failure to establish that Bennett discloses the first and fourth limitations of claim 43, the court does not reach whether Bennett discloses the second and third limitations of the claim. Nonetheless, the court notes that Rambus's argument with respect to the second input receiver circuitry appears misplaced. Rambus argues that Bennett does not anticipate claim 43 because Bennett does not disclose "programmable write delay." Claim 43's third limitation recites "input

receiver circuitry to sample data, in response to the operation code, after a predetermined number of clock cycles of the external clock." The claim says noting about varying the predetermined number of clock cycles or storing/programming the number of clock cycles in a register.

E. Claim 16 of the '863 Patent

1. The Asserted Claim

The Manufacturers also assert that the Bennett patent anticipates claim 16 of U.S. Patent No. 6,452,863. The claim generally recites a method of operating a synchronous memory device. The method generally involves (1) the device receiving and "processing" some block size information from a memory controller; (2) synchronously receiving a request for a write operation from the memory controller; and (3) inputting data in response, both synchronously and over more than one clock cycle. Rambus colloquially refers to this claim as covering the implementation of programmable or variable burst length. The full text of the claim follows:

> [[A method of operation in a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises:
>
> receiving first block size information from a memory controller, wherein the memory device is capable of processing the first block size information, wherein the first block size information represents a first amount of data to be input by the memory device in response to an operation code;
>
> receiving the operation code, from the memory controller, synchronously with respect to an external clock signal; and
>
> inputting the first amount of data in response to the operation code]]
>
> [wherein inputting the first amount of data includes receiving the first amount of data synchronously with respect to the external clock signal]
>
> wherein the first amount of data is sampled over a plurality of clock cycles of the external clock signal.

2. The Evidence With Respect to Each Limitation

a. Memory Device

The preambulary "memory device" limitation essentially mirrors that in claim 16 of the '285 patent. The court previously discussed the arguments regarding the Manufacturers' showing that the Bennett patent discloses a "memory device." *See supra* § III-B-2-a. The only difference in the two

"memory device" limitations is that claim 16 of the '863 patent adds a "synchronous" aspect to the limitation. The court determined that Bennett discloses synchronous memory devices in its prior discussion. *See supra* § III-B-2-b (discussing clock receiver circuitry).

b. Receiving Block Size Information

The method of claim 16 of the '863 patents begins with the memory device receiving block size information from a memory controller. "Block size information" means "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request."

Mr. McAlexander states that the Bennett patent discloses receiving block size information from a memory controller. *See* Bennett Chart, C-30. Mr. McAlexander points to two instances where he states that the memory device receives block size information. One does not disclose receiving block size information. The other does.

First, the Manufacturers and Mr. McAlexander point to the use of the BUSY signal in the block read and write operations defined by the Bennett inventors and discussed above. But the Manufacturers fail to show how the block read or write operations involve the memory device receiving block size information. On the contrary, the memory devices engaged in block operations in the Versatile Bus interface *never* receive information that specifies the total amount of data to be transferred. The memory devices receive only a request to begin a block operation and the BUSY signal from the master device. The block operation continues indefinitely until the master terminates the BUSY signal. The BUSY signal does not specify a total amount of data to be transferred; it only instructs the DRAM to continue to operate. In pursuing this argument, the Manufacturers lose sight of the difference between block memory operations and the memory device's receipt of block size information. The two are not the same.

The Manufacturers next argue that the Bennett memory device receives block size information when it receives parameters VII and VIII during configuration. As discussed, parameters VII and VIII define what the Bennett inventors call "data format." The parameters do not define the length of a block operation. The parameters simply define the dimensions of a single

data word. Thus, parameters VII and VIII cannot specify the total amount of data that will be transferred in response to a block read or block write operation. But they do specify the total amount of data to be transferred in response to Bennett's basic, single-word read or write operations.

Rambus argues that the fallacy in the Manufacturers' argument is that "the bits they point to do not specify the *number* of data words to be transferred." But the court's construction of "block size information" – "information that specifies the total amount of data that is to be transferred on the bus in response to a transaction request" – does not require the information to specify the number of data words. It only requires the information to specify the *total* amount of data to be transferred. Indisputably, parameters VII and VIII specify the total amount of data that will be transferred in response to two basic types of transaction requests.

And even if "block size information" had to specify the number of data words to be transferred, Bennett's parameters VII and VIII do to the same extent that the Farmwald/Horowitz specification's BlockSize[0:3] does. In the preferred embodiment interface of Drs. Farmwald and Horowitz, the block size parameter instructed the DRAM to send or receive 0-7, 8, 16, 32, 64, 128, 256, 512, or 1,024 bits of information. *See* U.S. Patent No. 6,426,916, col. 11, ll. 44-67. The preferred embodiment used eight bus data lines. Thus, when the DRAM received block size information, that information also specified the number of data words that would be transferred as well, i.e., 0-7 specified that no complete data words would be transferred, 8 specified that one data word would be transferred, 16 specified that two, and so on. Analogously, when Parameter VII equals VIII, the two parameters "specify" that one data word will be transferred in response to basic read and write operations.

There is another wrinkle, however. Unlike Rambus's other asserted claims, Claim 16 explicitly requires the presence of a memory controller. Specifically, the method of claim 16 requires the memory device to receive the block size information "from a memory controller." In Bennett's Versatile Bus interface, Parameters VII and VIII come from the maintenance processor. Mr. McAlexander does not state one way or the other whether Bennett's maintenance processor is a memory controller. *See* Bennett Chart, C-30. The court must therefore deny summary judgment

because the Manufacturers have failed to establish that Bennett anticipates claim 16 of the '863 patent by disclosing the memory device's receipt of block size information from a memory controller.

It is unclear whether the Manufacturers will be able to establish this at trial. To begin, the parties included "memory controller" among the terms on whose construction the parties could not agree. Joint Claim Construction Statement, Jt. App'x at 22. As with "memory array" though, the parties did not call this dispute to the court's attention during claim construction. Rambus submitted that a "memory controller" is "an integrated circuit device that includes circuitry to direct the actions of one or more memory device." *Id.* This broad construction of the term might encompass the maintenance processor because Bennett's maintenance processor dictates the "data format" of all future memory operations. It does not appear, however, that the maintenance processor directs any other actions of the memory device, i.e., the maintenance processor does not send requests for read or write operations to the memory devices in the Versatile Bus environment. On the other hand, the court cannot adopt the constructions proposed by the Manufacturers. Some Manufacturers proffered constructions incorporating the request packet limitation that the court has rejected. *See Rambus Inc. v. Hynix Semiconductor, Inc.*, 569 F. Supp. 2d 946, (N.D. Cal. 2008). Another did not offer a proposed construction because no claim asserted against that Manufacturer included a "memory controller" limitation at that time. Joint Claim Construction Statement, Jt. App'x at 22. Whether the parties still dispute the construction of the term "memory controller" and whether the Bennett maintenance processor is such a "memory controller" remain to be seen.

F. Claim 28 of the '916 Patent

Finally, the Manufacturers also move for summary judgment that the Bennett patent anticipates claim 28 of U.S. Patent No. 6,426,916. The claim generally recites a synchronous memory device that receives block size information and stores a value that is "representative" of a write latency period. The court previously discussed the Manufacturers' failure to carry their burden of persuasion with respect to the write latency limitation. *See supra* § III-B-2-d. Accordingly, the court denies the Manufacturers' motion for summary judgment with respect to claim 28 as well.

IV. ORDER

For the foregoing reasons, the court grants Rambus's motion to strike the Manufacturers' summary judgment motion no. 2 and the court does not consider it. The court denies Rambus's motion to strike the Manufacturers' summary judgment motion no. 1. The court denies the Manufacturers' motion for summary judgment no. 1.

DATED: 12/15/2008

Ronald M. Whyte

RONALD M. WHYTE
United States District Judge

Notice of this document has been electronically sent to counsel in:

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Dated: 12/15/2008

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